GENERAL INSTRUMENT
MOS INTEGRATED CIRCUIT

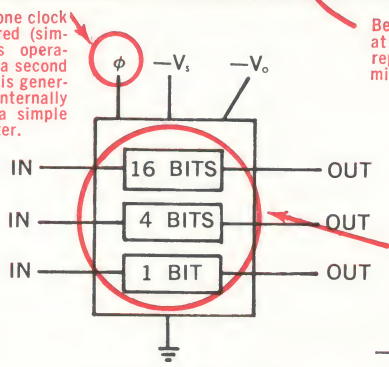
Technical Specifications
May, 1965

MEM 501

MOGISTER™...21-BIT MICROELECTRONIC MOS SHIFT REGISTER

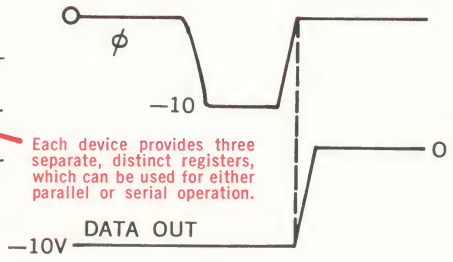
Only one clock required (simplifies operation); a second clock is generated internally with a simple inverter.

Because MOGISTERS turn on at 4V Typ., the user is assured of at least 3V noise immunity over the specified Temp. range. This represents an advantage of 2V minimum over any double-diffused microcircuit available.



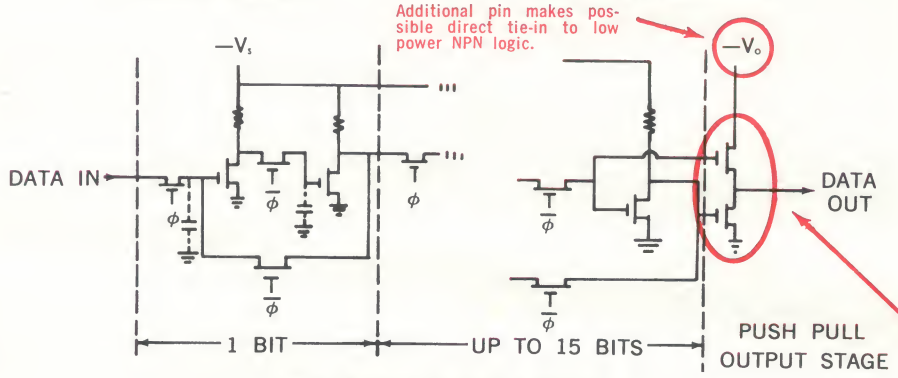
Each device provides three separate, distinct registers, which can be used for either parallel or serial operation.

Functional diagram



Timing relationship

Additional pin makes possible direct tie-in to low power NPN logic.



Circuit diagram of one channel

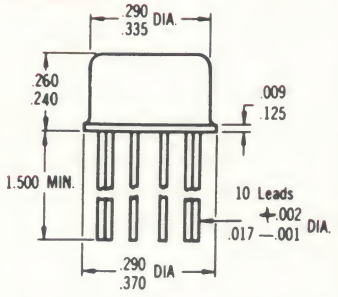
OPERATING CONDITIONS AND MAXIMUM RATINGS
(T_A = 25°C., UNLESS OTHERWISE SPECIFIED)

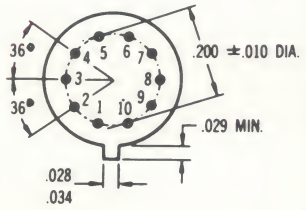
Power consumption	<150 mw
Supply voltage ($-V_s$)	−28 volts
Output supply voltage ($-V_o$)	0 to −28 volts
Shift pulse amplitude (ϕ)	0 to ≤ −10 volts
Shift pulse frequency	DC to 500 KC
Shift pulse rise and fall times (t_r, t_f)	<100 nsec
Shift pulse width (t_w) (to 50% points)	400 nsec < t_w < 50 μsec
Shift pulse input impedance	6 pf, 50 kΩ
Input swing	0 to ≤ −10 volts
Output swing (no dc load)	0 to ≤ −12 volts
Input capacitance	2 pf
Output impedance	<2 kΩ at ground <10 kΩ at −10 volts
Operating temperature	−55°C to 125°C military −55°C to 85°C commercial

Very conservative rating. MOGISTERS will actually operate at −190°C.

10 LEAD TO-5 TYPE PACKAGE

Also available in ¼" x ⅜" flat pack (MEM501F).





Bottom view of 10 lead header

Note: All dimensions in inches

Each stage incorporates a push-pull output, which increases speed and permits working into impedances as low as 2 kΩ.

TERMINALS

Lead

1. Input (16 Bit)
2. φ (Clock)
3. Output Supply Voltage $-V_o$
4. Output (16 Bit)
5. Ground
6. Output (4 Bit)
7. Output (1 Bit)
8. Input (1 Bit)
9. Input (4 Bit)
10. Supply Voltage $-V_s$

Permits user to stop clock input at any time. Unit will store information indefinitely between shift pulses (each bit is actually a cross-coupled flip-flop).

21-BIT SHIFT REGISTER

MEM 501

TENTATIVE SPECIFICATIONS

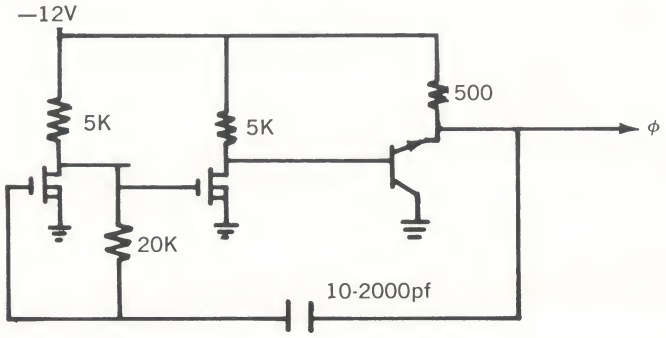
The G.I. 21 bit shift register is really 3 shift registers in one package sharing common supply and clock voltages. The three can be used either independently or connected in series to give a total of 21 bits of delay to an arbitrary data stream.

Each bit of delay has a cross-coupled flip-flop, in order that data might be stored indefinitely between shift pulses. Only a single phase shift pulse ϕ has to be supplied; the additional 180° out of phase pulse ϕ is generated by an inverter in the chip.

The outputs will change on the trailing edge of the shift pulse, i.e., when ϕ goes from −10 to 0 volts. However, there is sufficient built in delay so that an output won't start changing appreciably until the shift pulse is completely to zero, if the fall time of the shift pulse is less than 100 nsec. This delay makes it possible to transfer data from outputs of shift registers to inputs without any difficulty. In general, wherever data comes from to be fed to a shift register input, precautions should be taken to have the data not changing during the shift pulse fall time.

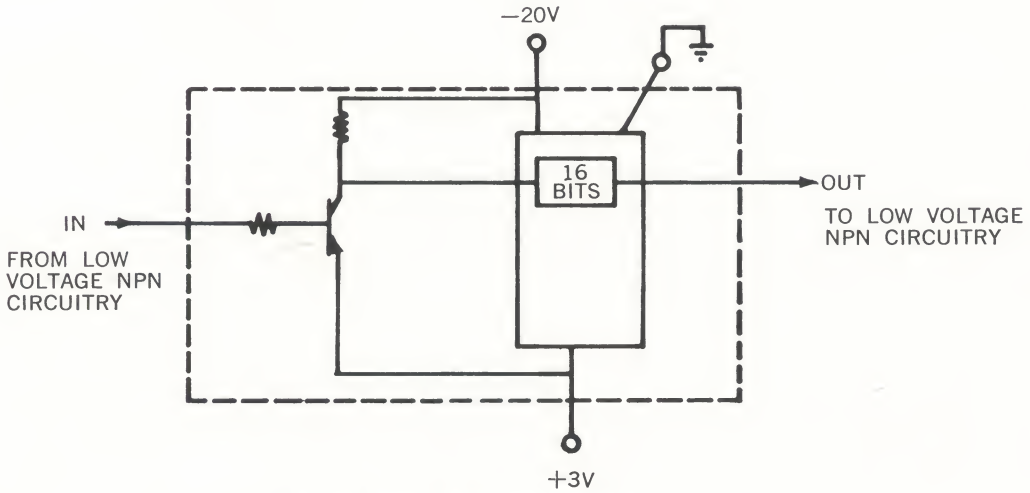
The supply voltage $-V_o$ for the output stages can have any value between ground and −22 volts. By letting $-V_o$ be just a few volts it is possible to have this shift register drive other types of low voltage NPN transistor logic.

The shift pulse can be regularly supplied from a clock generator as shown below or it may be supplied aperiodically through logic networks. The shift pulse amplitude requirement is the same as the logic swing required.



Shift pulse generator

It is possible to use the shift register with low voltage NPN transistor logic if desired by using the circuit below. However, it is more convenient to use the register with either MOS logic or large voltage swing PNP transistor logic.



Buffer circuit to interface NPN logic

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